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10/041,671	01/10/2002	Allon Adir	ADIR2	2977

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EXAMINER	
PATEL, SHAMBHAVI K	

ART UNIT	PAPER NUMBER
2128	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/041,671	ADIR, ALLON	
	Examiner	Art Unit	
	SHAMBHAVI PATEL	2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *10 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-70* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-70* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *05/08/02*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-70 have been presented for examination.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 08 May 2002 is in compliance with the provisions of 37 CFR 1.97. Accordingly, the Examiner has considered the IDS as to the merits.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. **Claims 4-5, 7, 11-13, 17-20, 30, 31, 33, 37, 38, 39, 43-45, 48, 50, 51, 57, 61-64, 66, 67, 69 and 70 are rejected under 35 U.S.C.112, second paragraph, as being indefinite** for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Regarding **claims 4 and 30**, the term "value-list" is vague and indefinite. Regarding **claims 5 and 31**, the term "adjacent resources" is vague and indefinite. Regarding **claims 7, 33 and 57,** the term "common combination identifier" is vague and indefinite. Regarding **claims 11, 37 and 61**, it is unclear how the simulated of said generated instruction can be performed while the step of generating the instruction is also performed (2nd limitation). Regarding **claims 17, 43 and 66,** the term "adjacent resources" is vague and indefinite. Regarding **claims 20, 48 and 67,** the terms "mutually dependent non-adjacent resources", "value lists" and "unique combination identifier" are vague and indefinite. Regarding **claims 24, 50 and 69** the term "process-linked lists" is vague and indefinite. Regarding **claims 39 and 63,** the limitations "identifying a first unique combination of said first simulated process and said first read values" and "identifying a second unique combination of said simulated process and said second read values" and "using a selected value" are vague and indefinite. What is a "unique combination"? How is it identified? How is the value selected? Regarding **claims 51, 64, and 70,** the terms "process-linked lists", "unique value" and "associated process" are vague and indefinite. All other claims are rejected by virtue of their dependency.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

4. Claims 1-70 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter. The Examiner asserts that the current state of the claim language is such that a reasonable interpretation of the claims would not result in any useful, concrete or tangible product. The claims are directed to a method for validating a processor design by simulating program execution **(claim 1),** a method of verification of an architecture by simulation **(claim 16),** a method of predicting non-unique results by simulating a system design **(claim 21),** a computer software product for validating a computer process design by simulating program execution **(claim 27),** a computer software product for performing a method of verification of an architecture by simulation **(claim 42),** a computer program product for performing a method of predicting non-unique results by simulating a system design **(claim 49),** an apparatus for verifying a design comprising a simulation apparatus **(claim 52),** an apparatus for verifying an architecture by simulation comprising a simulation processor **(claim 65),** and an apparatus for design verification **(claim 68)**. The claimed subject matter does not produce a tangible result because the claimed subject matter fails to produce a result that is limited to having real world value rather than a result that may be interpreted to be abstract in nature as, for example, a thought, a computation, or manipulated data. More specifically, the claimed subject matter provides for verifying an equality between a content of a resource and a member of a set of non-unique values **(claims 1, 27 and 52),** verifying an actual resource result by determining that at least on of a plurality of permissible results is equal to said actual resource result **(claims 16, 42 and 65),** calculating possible values of target resources of a single instruction **(claims 21, 49 and 68)**. These produced results remain in the abstract and, thus, fail to achieve the required statuses of having real world values.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-70 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by **Genie ("Genesys-MP: User's Guide).**

Regarding claims 1, 27 and 52:

Genie discloses a method for validating a processor design by simulating program execution, comprising the steps of

a. identifying a resource that may be accessed by a test program that includes a first simulated process and a second simulated process **(figure 1 "shared memory")**

b. associating a set of non-unique values for said resource **(section 2.11: 2nd paragraph: group of results for all possible orders in which instructions are interleaved)**

c. executing said test program by executing a first sequence of instructions in said first simulated process and while performing said step of executing said first sequence, executing a second sequence of instructions in said second simulated process **(section 2.11.1: command for executing test cases)**

d. wherein said resource is accessed by at least one of said first simulated process and said second simulated process **(section 2.11: two processes can access the same memory at the same time)**, and wherein upon completion of said steps of executing said first sequence and executing said second sequence, a member of said set of non-unique values is required to be present in said resource **(section 2.11: group of possible results)**

e. verifying an equality between a content of said resource and a member of said set of non-unique values **(section 2.11.5: testcase)**

Regarding claims 2, 28 and 53:

Genie discloses the method according to claim 1, wherein said resource is a memory resource **(figure 1: shared memory)**

Regarding claims 3, 29 and 54:

Genie discloses the method according to claim 1, wherein said resource is a register **(section 2.1.5 "memory sharing rules": register)**

Regarding claims 4 and 30:

Genie discloses the method according to claim 1, wherein said set of non-unique values is a set of value-lists **(section 2.11.5 "multiple results cards")**.

Regarding claims 5 and 31:

Genie discloses the method according to claim 4, wherein said resource comprises a first adjacent resource and a second adjacent resource **(figure 1: shared memory contains multiple registers; section 2.1.5)**, and each member of said set of value-lists comprises a first value and a second value **(section 2.11.5 "multiple results cards")**, said first value being a permissible value of said first adjacent resource, and said second value being a permissible values of said second adjacent resource **(section 2.11.5 "multiple results cards": possible results)**, and verifying further comprising identifying a valid member of said set of value-lists, by verifying an equality between a content of said first and second adjacent resource and said first and second value of said valid member **(section 2.11.5: testcase)**

Regarding claims 6, 32 and 56:

Genie discloses the method according to claim 1, wherein said resource comprises a first resource and a second resource **(figure 1: shared memory contains multiple registers; section 2.1.5)** and said set of non-unique values comprises a first set of non-unique values that is associated with said first resource, and a second set of non-unique values that is associated with said second resource **(section 2.11.5 "multiple results cards")**, further comprising associating a first member of said first set of non-unique values with a second member of said second set of non-unique values **(sections 2.11.3 and 2.11.4: collisions)**; and verifying an equality between said first resource and said first member; and verifying an equality between said second resource and said second member **(section**

2.11.5: testcase).

Regarding claims 7, 33, and 57:

Genie discloses the method according to claim 6, wherein said step of associating said first member is performed by tagging said first member and said second member with a common combination identifier **(section 2.11.3: results contained in same list)**.

Regarding claims 8, 34 and 58:

Genie discloses the method according to claim 6, said first member of said first set of non-unique values comprises a first value-list, and said second member of said second set of non-unique values comprises a second value-list **(section 2.11.5 "multiple results cards")**, respective elements of said first value-list being permissible values of said first resource and adjacent resources thereof, and respective elements of said second value-list being permissible values of said second resource and adjacent resources thereof **(section 2.11.5 "multiple results cards": possible results)**, verifying an equality between a content of said first resource and adjacent resources thereof with corresponding elements of said first value-list; and verifying an equality between a content of said second resource and adjacent resources thereof with corresponding elements of said second value-list **(section 2.11.5: testcase)**.

Regarding claims 9, 35 and 59:

Genie discloses the method according to claim 1, wherein said step of associating said set of non-unique values is performed prior to said step of executing said first sequence of instructions **(section 2.11.5 "multiple results cards")**.

Regarding claims 10, 36 and 60:

Genie discloses the method according to claim 9, further comprising the steps of: defining a results section in said test program, and entering all permissible values assumable by said resource and an identifier of said resource in an entry of said results section **(section 2.11.5 "multiple results cards": all possible result values)**.

Regarding claims 11, 37 and 61:

Genie discloses the method according to claim 1, wherein said step of executing said test program further comprises the steps of: generating said first sequence and said second sequence to define generated instructions **(section 3.5)** while performing said step of generating, simulating one of said generated instructions in said first simulated process and said second simulated process **(section 2.11.1: command for executing test cases)** maintaining a store that contains a set of values that are assumable in said resource during said step of simulating said one of said generated instructions **(section 2.11.5 "multiple results cards")** and thereafter determining whether said store contains non-unique values **(section 2.11.5: testcase)**.

Regarding claims 12, 38 and 62:

Genie discloses the method according to claim 11, further storing in said store first values of said resource during accesses thereof by said first simulated process and storing in said store second values of said resource by said second simulated process during accesses thereof **(section 2.12: processor 1 and processor 2)**, wherein said first values comprise first written values, and said second values comprise second written values **(section 2.12: instructions store load)** and; identifying in said store a last value written to said resource in said step of simulating said one of said generated instructions **(section 2.12: instructions)**.

Regarding claims 13:

Genie discloses the method according to claim 11, wherein said step of maintaining said store further comprises the steps of determining an initial state of said test program immediately prior to performing said step of simulating said one of said generated instructions **(section 3.1 configuration)**, storing in said store written values of target resources of said one generated instruction during accesses thereof **(section 3.5: write)** and identifying all combinations of values of input resources of said one generated instruction **(section 2.11.5 "multiple results cards": possible results)**, rolling back said test program to reestablish said initial state **(section 3.1 configuration)**, thereafter resimulating said one of said generated instructions using each of said combinations of values **(section 2.11.1: command for executing test cases),** reidentifying written values that are written to said target resources

(section 3.5: write); and updating said store with reidentified written values of said target resources **(section 2.11.5: testcase)**.

Regarding claims 14, 40:

Genie discloses the method according to claim 1, further comprising the step of establishing a synchronization barrier for said first simulated process and said second simulated process **(section 2.9 synchronization protocol)**.

Regarding claims 15, 41:

Genie discloses the method according to claim 1, further comprising the steps of biasing generation of said test program to promote collisions of memory accessing instructions that are executed by said first simulated process and said second simulated process **(section 2.13: memory biasing)**.

Regarding claims 16, 42 and 65:

Genie discloses a method of verification of an architecture by simulation, comprising the steps of:

a. defining a program input to a test generator **(section 2.1 file)**

b. generating a test program responsive to said program input **(section 3.1)** said test program including a list of resource initializations **(section 3.1 processor)**, a list of instructions **(sections 2.11.3 and 2.11.4: collisions)**, and a list of predicted resource results, wherein at least one member of said list of predicted resource results comprises a plurality of permissible results **(section 2.11: group of possible results)**

c. simulating an execution of said test program using a plurality of simultaneously executing processes **(section 2.11: two processes can access the same memory at the same time)**

d. verifying an actual resource result by determining that at least one of said plurality of permissible results is equal to said actual resource result **(section 2.11.5: testcase)**

Regarding claims 17, 43 and 66:

Genie discloses the method according to claim 16, wherein said list of predicted resource results comprises predicted results of adjacent resources, wherein said adjacent resources are mutually dependent, and said step of verifying said actual resource result is performed by verifying each of said adjacent resources **(figure 1: shared memory contains multiple registers; section 2.1.5)**.

Regarding claims 18 and 44:

Genie discloses the method according to claim 17, wherein said adjacent resources are memory resources **(figure 1: shared memory)**.

Regarding claims 19 and 45:

Genie discloses the method according to claim 17, wherein said adjacent resources are registers **(section 2.1.5 "memory sharing rules": register)**.

Regarding claims 20, 48 and 67:

Genie discloses the method according to claim 16, wherein said list of predicted resource results comprises predicted results of mutually dependent non-adjacent resources **(section 2.11.5 "multiple results cards": possible results)**, further identifying a combination of said mutually dependent non-adjacent resources by tagging corresponding members of said list of predicted resource results with a unique combination identifier to define commonly tagged value-lists of predicted resource results **(section 2.11.3: results contained in same list)**; and said step of verifying said actual resource result is performed by verifying that resources of said combination have actual results that are equal to a member of a corresponding one of said commonly tagged value-lists **(section 2.11.5: testcase)**.

Regarding claims 21, 49 and 68:

Genie discloses a method of predicting non-unique results by simulating a system design, comprising the steps of:

a. defining a program input to a test generator **(section 2.1 file)**

b. generating a test program responsive to said program input**(section 3.1)** said test program including a list of resource initializations **(section 3.1 processor)**, a list of instructions **(sections 2.11.3 and 2.11.4: collisions)**, and a list of predicted resource results, wherein at least one member of said list of predicted resource results comprises a plurality of permissible results **(section 2.11: group of possible results)**

c. simulating an execution of a single instruction of said test program by a first process of said test program **(section 2.11: instruction simulation)**

d. calculating possible values of target resources of said single instruction **(section 2.11.5: testcase)**

Regarding claims 22:

Genie discloses the method according to claim 21, wherein said target resources are memory resources **(figure 1: shared memory)**.

Regarding claims 23:

Genie discloses the method according to claim 21, wherein said target resources are registers **(section 2.1.5 "memory sharing rules": register)**.

Regarding claims 24, 50 and 69:

Genie discloses the method according to claim 21, further comprising the steps of: performing said step of simulating an execution by a second process of said test program **(section 2.11.1: command for executing test cases),** maintaining process-linked lists of written values that are written to said target resources of said single instruction by said first process and said second process **(section 3.5: write)**; and determining respective last values in said process-linked lists of written values **(section 2.11.5: testcase)**.

Regarding claims 25, 46:

Genie discloses the method according to claim 16, further comprising the step of establishing a synchronization barrier for said simultaneously executing processes **(section 2.9 synchronization protocol)**.

Regarding claims 26, 47:

Genie discloses the method according to claim 1, further comprising the steps of biasing generation of said test program to promote collisions of memory accessing instructions that are executed by said first simulated process and said second simulated process **(section 2.13: memory biasing)**.

Regarding claims 39 and 63:

Genie discloses the computer software product according to claim 38, the method further comprising the steps of:

a. identifying a first unique combination of said first simulated process and said first read values **(section 3.6 read-write collision between two processes)**
b. identifying a second unique combination of said second simulated process and said second read values **(section 3.6 read-write collision between two processes)**
c. resimulating of said generated instructions using a selected value that is selected from said first read values and said second read values as an input to said one of said generated instructions **(section 2.11.1: command for executing test cases)**
d. reidentifying values that are written to said resource in said step of resimulating **(section 3.5: write)**

Regarding claims 51, 64 and 70:

Genie discloses the computer software product according to claim 50, the method further comprising the steps of:

a. prior to performing said steps of simulating said execution by said first process and of simulating said execution by said second process memorizing an initial simulated state of said test program **(section 3.1 configuration)**
b. maintaining process-linked lists of read values that are read from source resources of said single instruction **(section 3.5: write)**

c. identifying a member of said lists of read values having a unique value to define an identified member **(section 2.11.5: testcase)**

d. restoring said initial simulated state of said test program **(section 3.1 configuration)**

e. performing said step of simulating said execution a second time, reading said identified member, using an associated process thereof **(section 2.11.1: command for executing test cases)**

Regarding claim 55:

Genie discloses the apparatus according to claim 52, wherein said resource comprises a first adjacent resource and a second adjacent resource **(figure 1: shared memory contains multiple registers; section 2.1.5)**, and said set of non-unique values comprises a first subset of non-unique values and a second subset of non-unique values **(section 2.11.5 "multiple results cards")**, said first subset of non-unique values being permissible values of said first adjacent resource, and said second subset of non-unique values being permissible values of said second adjacent resource **(section 2.11.5 "multiple results cards": possible results)**, establishing at least one allowable subcombination of members of said set of non-unique values, a first member of said subcombination being selected from said first subset of non-unique values and a second member of said subcombination being selected from said second subset of non-unique values **(section 2.11.3: list of non-unique results)** and verifying an equality between a content of said first adjacent resource and said first member of said subcombination; and verifying an equality between a content of said second adjacent resource and said second member of said subcombination **(section 2.11.5: testcase)**

Conclusion

6. **Examiner's Remarks:** Examiner has cited particular columns and line numbers in the references applied to the claims above for the convenience of the applicant. Although the specified citations are representative of the teachings of the art and are applied to specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested from the applicant in preparing responses, to fully consider the references in their entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art or disclosed by the Examiner. In the case of amending the claimed invention, Applicant is respectfully requested to indicate the portion(s) of the specification which dictate(s) the structure relied on for proper interpretation and also to verify and ascertain the metes and bounds of the claimed invention.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shambhavi Patel whose telephone number is (571) 272-5877. The examiner can normally be reached on Monday-Friday, 8:00 am – 4:30 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamini Shah can be reached on (571) 272-2279. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SKP

/Kamini S Shah/
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